

**Amendment/Reply**

Applicant: Andrew Graham et al.

Serial No.: 10/533,550

Filed: November 17, 2005

Docket No.: I432.116.101/P29858

Title: VERTICALLY INTEGRATED FIELD-EFFECT TRANSISTOR

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**REMARKS**

This Amendment/Reply accompanies the Request for Continued Examination (RCE) 37 CFR 1.114 and is in reply to the Final Office Action mailed September 18, 2008. Claims 43 and 45 have been withdrawn from consideration. Claims 22-25, 27-37, 39-42, and 44 were rejected. With this Response, claims 22, 41, and 44 have been amended. Claims 22-25, 27-37, 39-42, and 44 remain pending in the application and are presented for reconsideration and allowance.

**In the Specification**

The Examiner objected to the title of the invention asserting that the title is not descriptive. Applicants have amended the title to correct this asserted informality. Applicants believe the title is now in condition for allowance.

**Claim Rejections under 35 U.S.C. § 112**

The Examiner rejected claims 22, 41, and 44 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement, asserting that the claims contain subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claim invention. With this response, Applicants have deleted the portions objected to by the Examiner. As such, the portions of the claims subjected to the rejection are no longer in the case.

In view of the above, claims 22, 41, and 44 are believed to be in form for allowance. Therefore, Applicants respectfully request that rejections to these claims under 35 U.S.C. § 112, first paragraph, be reconsidered, and that the rejections be removed and these claims be allowed.

**Claim Rejections under 35 U.S.C. § 102**

The Examiner rejected claims 22, 33-35, 40-41, and 44 under 35 U.S.C. § 102(e) as being anticipated by the Farnworth et al. U.S. Patent No. 6,515,325. As amended, the claims are not taught or suggested by the Farnworth reference or the art of record.

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As amended, claim 22 is a vertically integrated field-effect transistor including a first electrically conductive layer, a middle layer formed partially from dielectric material on the first electrically conductive layer, and a second electrically conductive layer on the middle layer. A nanostructure is *vertically grown up in a via hole from the bottom of the via hole* introduced into the middle layer. The nanostructure further includes a first end portion that is coupled to the first electrically conductive layer and a second end portion that is coupled to the second electrically conductive layer. The first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region of the field-effect transistor. The middle layer, between two adjacent dielectric sublayers, has a third electrically conductive layer, the thickness of which is less than the thickness of at least one of the dielectric sublayers. A ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein. This is not taught or suggested in the Farnworth reference or the art of record.

As amended claim 22 includes a nanostructure is *vertically grown up in a via hole from the bottom of the via hole* introduced into the middle layer. Support for the amendment is found at least in Figure 1A and paragraphs [0023] and [0026] of the specification of the published application (US 2006/0128088 A1). As provided in paragraph [0023], the nanostructure can be grown up vertically in a via hole. Further, as provided in paragraph [0026], the catalyst for growing up the nanostructure is arranged on the first conductive layer, which is, as can be seen from Figure 1A, the bottom of the via hole. This feature is not taught or suggested in the art of record.

Specifically, the Farnworth reference does not disclose that a nanostructure is grown up in a via hole from the bottom of the via hole. In fact, the Farnworth reference merely discloses (in connection with related embodiments) that an insulating layer is formed (deposited) over a pre-grown nanotube (*see*, col. 5, lines 29 to 34 and Figure 2G; and *see*, col. 7, lines 1 to 3 and Figure 4C). Growing up the nanostructure in the via hole makes it possible to implement the nanostructure without the danger of destruction of the nanostructure by a subsequent deposition

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process. This is not the case for the structure disclosed by the Farnworth reference, which teaches use of subsequent deposition process, thereby involving the danger of destruction of the nanostructure.

Furthermore, the nanostructure grown up in the via hole from the bottom of the via hole as claimed by the amended claims results in a region in the via hole between the nanostructure and the respective dielectric sublayer, which is free of electrically insulating material. In the field-effect transistor device 70 shown in Figure 5 of the Farnworth reference, the sub regions of insulating layer 20 above, below and between gates 79 and 81 are formed directly on the nanotube 22. That is, there is no region free of electrically insulating material left in the via hole between nanostructure 22 and the insulating material of layer 20 within regions A, C and E.

As such, the transistor according to the amended claim is not taught or suggested in the Farnworth reference, which actually leads the person skilled in the art to a transistor having a different structure. As such, claim 22, and claims 41 and 44, which include similar features, are allowable over the Farnworth reference and the art of record. Because claims 33-35 and 40 ultimately depend from claim 22, these claims are also in condition for allowance. Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 102(e) rejection to the claims, and request allowance of these claims.

**Claim Rejections under 35 U.S.C. § 103**

The Examiner rejected claims 22-25, 27-28, and 30-43 under 35 U.S.C. § 103(a) as being unpatentable over the Mancevski U.S. Patent Application Publication No. 2001/0023986 in view of the Choi et al. U.S. Patent Application Publication No. 2002/0001905.

The Examiner rejected claim 29 under 35 U.S.C. § 103(a) as being unpatentable over the Mancevski U.S. Patent Application Publication No. 2001/0023986 in view of the Martin et al. U.S. Patent Application Publication No. 2001/0019279. As amended, the claims are not taught or suggested by the Mancevski, Choi, or Martin references.

The Mancevski reference fails to disclose the nanostructure grown up from the bottom of the via hole. As it can be seen in Figure 3 of the Mancevski publication, the catalyst is deposited on the side walls of an etched cavity. Hence, the nanostructure according to the Mancevski

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reference is not grown up from the bottom of a via hole, quite the contrary, it is formed beginning from the side walls, probably in a horizontal direction.

Furthermore, it is clear that using the very oppositional forming process of the Mancevski reference does not make it possible to implement a nanostructure, wherein a region in the via hole between the nanostructure and the respective dielectric sublayer, which is free of electrically insulating material, which can be the case for the nanostructure according to amended claims 22 and 41, since the direction of growth in the Mancevski reference is horizontal from the side walls, which precludes the possibility of a region in the via hole between the nanostructure and the respective dielectric sublayer, which is free of electrically insulating material.

Furthermore, the Mancevski reference fails to disclose the electrically insulating ring structure as gate-insulating region of the field-effect transistor, arranged in a third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein, wherein the third electrically conductive layer is arranged between two adjacent dielectric sublayers. In fact, the Mancevski reference neither discloses nor suggests to provide any gate-insulating region at all.

The Choi reference discloses a vertical field-effect transistor (Figure 1) having a carbon nanotube 100 as a channel arranged on a source layer 40 and a nonconductor film 30 that electrically insulates the nanotube 100 from a gate 20 of the transistor. In contrast to the transistor according to amended claims, the nonconductor film 30 is deposited on the nanotube 100 thereby filling the entire region 10' with electrically insulating material of the non-conductor film 30. The nanotube 100 abuts the non-conductor layer 30 such that there is no region free of electrically insulating material left between the nanotube 100 and non-conductor film 30. Consequently, the danger of destruction of the nanostructure by filling the entire region 10' with the nonconductor film 30 is very high.

But this problem of the Choi reference is solved by the transistor according to amended claims, wherein a nanostructure vertically is grown up in a via hole from the bottom of the via hole introduced into the middle layer and wherein a ring structure is formed from an electrically insulating material as gate-insulating region of the field-effect transistor and is arranged in the third electrically conductive layer, which makes it possible to isolate the

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nanostructure from the gate without the need of filling the via hole with an insulating material as it is the case in the Choi reference, which would lead to a high risk of defects of the nanostructures.

Fiannly, the Martin reference merely discloses a method and an apparatus for reducing induced switching transients. However, the Martin reference is completely silent regarding the integration of a nanostructure in a transistor. The Martin reference therefore fails to cure the above-mentioned deficiencies of the Mancevski reference.

As such, claims 22, 41 and 44 are allowable over the Mancevski reference in view of Choi reference and over the Mancevski reference in view of the Martin reference for at least the reasons given above. In view of the foregoing, reconsideration and allowance of claims 22-25, 27-37, 39-42, and 44 are solicited. Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection to the claims, and request allowance of these claims.

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**CONCLUSION**

In view of the above, Applicant respectfully submits that pending claims 22-25, 27-37, 39-42, and 44 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 22-25, 27-37, 39-42, and 44 are respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Paul P. Kempf at Telephone No. (612) 767-2502, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

**Dicke, Billig & Czaja**  
Fifth Street Towers, Suite 2250  
100 South Fifth Street  
Minneapolis, MN 55402

Respectfully submitted,

Andrew Graham et al.,

By their attorneys,

**DICKE, BILLIG & CZAJA, PLLC**  
Fifth Street Towers, Suite 2250  
100 South Fifth Street  
Minneapolis, MN 55402  
Telephone: (612) 767-2502  
Facsimile: (612) 573-2005

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/paulpkempf/

Paul P. Kempf

Reg. No. 39,727